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A 0.5ps 1.4mW 50MS/s Nyquist Bandwidth Time Amplifier Based Two-Step Flash-ΔΣ Time-to-Digital Converter

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***Abstract*—We propose a 50-MS/s two-step flash-ΔΣ time-to-digital converter (TDC) using stable time amplifiers (TAs). The TDC demonstrates low-levels of shaped quantization noise. The system is simulated in 40-nm CMOS and consumes 1.3 mA from a 1.1 V supply. The bandwidth is broadened to Nyquist rate. At frequencies below 25 MHz, the integrated TDC error is as low as 143 fsrms, which is equal to an equivalent TDC resolution of 0.5 ps.**

***Index Terms*—Noise shaping, time domain register, error feedback, time-interleaved, time amplifier, two-step, TDC, MASH.**

I. Introduction

A time-to-digital converter (TDC) is one of the key elements for the digitalization of time information in modern mixed-signal circuits, such as all-digital PLLs, DLLs, ADCs and on-chip jitter monitoring. The resolution, linearity, dynamic range, and bandwidth of TDC have been major considerations in such applications.

To achieve both wide dynamic range and high resolution, two-step coarse-fine TDC has been recently introduced [1]. It improves the resolution in the second step by amplifying the time residue after the coarse conversion in the first step. However, as the time amplification utilizes the delay during metastability, the gain of the time amplifier (TA) suffers from small input range and nonlinearity. A noise-shaping TDC with a gated ring oscillator was another approach to improve effective resolution [2]. However, the multiphase generation and multiple counters consume large power, and the mismatches among multiple delay elements eventually limits the linearity performance.

The higher-order noise-shaping TDC was proposed in [3] to achieve high resolution and wide bandwidth. However, the high-order shaped noise needs to be filtered by the digital filter. This not only complicates the filter design but also limits the signal bandwidth.

To further improve the resolution, bandwidth and linearity, a new ΔΣ TDC architecture is proposed in this paper. The time amplifier is used between the 1st stage flash TDC and 2nd stage ΔΣ TDC to improve the time resolution. The TAs are also placed between each stage of MASH 1-1-1 TDC. The high-order quantization noise of the ΔΣ TDC can be largely reduced by the gain of TA. Meanwhile, the bandwidth of TDC is dramatically broadened to Nyquist bandwidth, Fs/2. The linearity is optimized by calibration. The proposed TDC can achieve sub-picosecond resolution with high linearity.

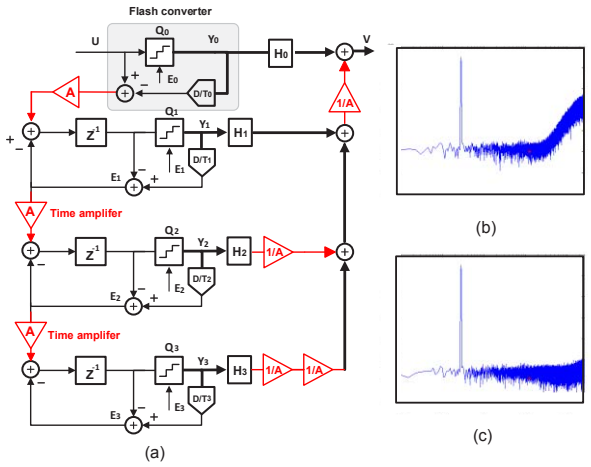

Fig. 1: The z-domain of two-step MASH 1-1-1 ΔΣ TDC model with ×8 TAs (a); PSD of output without TAs (b) and with TAs (c)

An overview of the paper is as follows. Section II describes the principle of proposed TA based flash-ΔΣ TDC. Section III details the circuit implementation. Section IV discloses the simulation results. Conclusions are drawn in Section V.

II. Principle of TA Based Two-Step Flash-ΔΣ TDC

A z-domain representation of the proposed TDC is shown in Fig. 1(a). It is made of the TAs, flash and ΔΣ converter stages. The multi-bit flash-converter coarsely estimates the time difference input yielding MSBs, Y_0, of the final TDC output code V. The digital-to-time converter (DTC_0) then converts the multi-bit signal back to the time-domain, which is then subtracted from the input to give the coarse quantization error or residue. Next, the residue is amplified by TA and then fed into the 2nd stage ΔΣ converter. The ΔΣ converter yielding the LSBs of the output code, is built in an error-feedback structure with TAs between each stages. The LSBs are scaled by 1/A in digital output to normalize the gain of time amplification. Assuming an ideal operation of DTCs and E_0=E_1=E_2=E_3, the coarse results (with unit delays) and the fine results can be added to obtain the final output as follows:

$$V = z^{-3}U + (1 - z^{-1})E_3/A^3 \qquad (1)$$

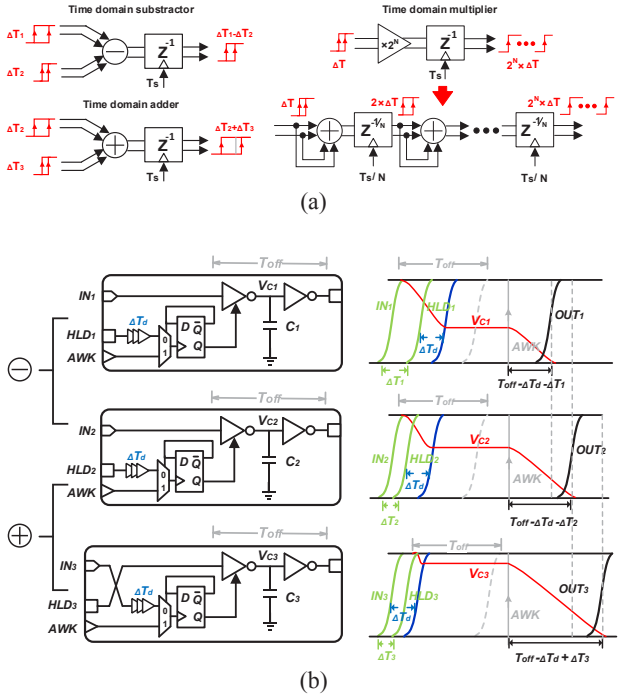

Fig. 2: Simplified block diagrams of time registered adder, subtractor and multiplier (a); and the operation principle of time adder/substractor (b).

It is noted that the quantization error from the 1st stage, E_0 does not appear at the output, *V*. Only E_3, the error introduced at the 3rd stage of ΔΣ TDC, contributes to the quantization noise of the two-step TDC (ignoring the noise sources inside the blocks). Thanks to the TAs, the quantization noise is further reduced by $1/A^3$. Assuming A=8, the quantization noise will be then reduced by 54dB. The Fig. 1(b) and Fig. 1(c) show the PSDs of TDC output without and with TAs, respectively. As it is expected, the quantization noise is invisible as it is reduced to below the level of device noise, such as flicker and thermal noise. Therefore, the signal bandwidth, which is usually severely limited by the quantization noise, can reach up to ½ of the sampling bandwidth.

Another benefit of the TA, which is located between 1st and 2nd stage TDCs, is to minimize the noise from the 2nd stage ΔΣ TDC. Theoretically, the noise is shrunk by the gain of TA.

III. Circuits Implementation

A. Time-domain signal processing

Fig. 2(a) introduces operational principles of the time-domain amplifier, which is designed with multiple time adders. The $\times 2^N$ amplification is realized by cascading *N*-stage time adders. The time adder of each stages receives two time differences as its input and produces two output

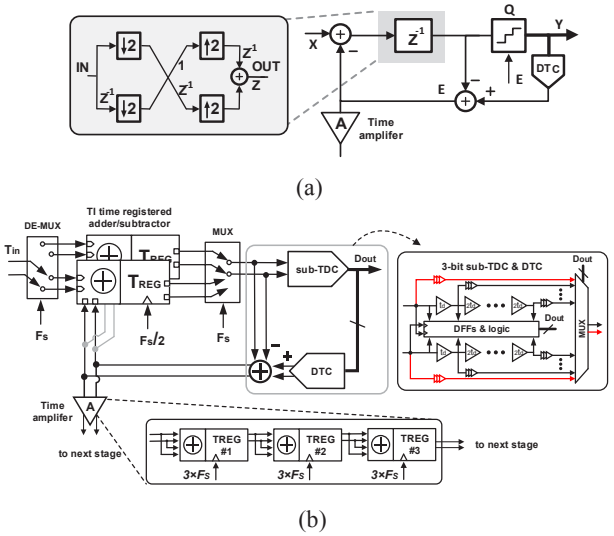

Fig. 3: z-domain model (a) and block diagram (b) of 1st order noise shaping error-feedback TDC.

edges whose relative time difference is the sum of the input time differences when a N×Fs sampling frequency is applied.

A key component of the time adder is a time register which is implemented using a tristate inverter with a trigged control circuit. As it is shown in Fig. 2(b). When the *IN* signal is initially low, the load capacitor is pre-charged to *VDD*. After the rising edge is applied to *IN*, the capacitor starts to discharge until the rising edge is later applied to *HLD*. The voltage *Vc* is held steady until a trigger edge *AWK* resumes its discharge. Thus, the rising edge of *IN* is eventually propagated to output *OUT*. In other words, if the input time difference is ΔT, the re-discharge time between *AWK* and *OUT* is $T_{off} - \Delta T$, where T_{off} is the whole discharging time of the buffer.

Two of such time registers can be implemented as a time substractor. When the time intervals ΔT_1 and ΔT_2 are applied to the inputs, the time difference of outputs is $\Delta T_1 - \Delta T_2$. A time adder can be realized if the inputs are swapped. The delay ΔT_d is added to make sure the *HLD* signal arrives after *IN*. Note that the proposed adder can be considered as a clocked adder due to the *AWK* signal. The proposed ×2 TA can be simply implemented by a time adder with applying time differences into two input operands.

B. Error feedback structure of TDC

Fig. 3(a) shows z-domain model of the 1st order ΔΣ TDC in the error-feedback configuration. It consists of a time-interleaved time registered subtractor, a multi-bits sub-TDC and a multi-bit DTC. The time-interleaved subtractor is implemented using two parallel identical units to provide the trade-off between accuracy and speed [4].

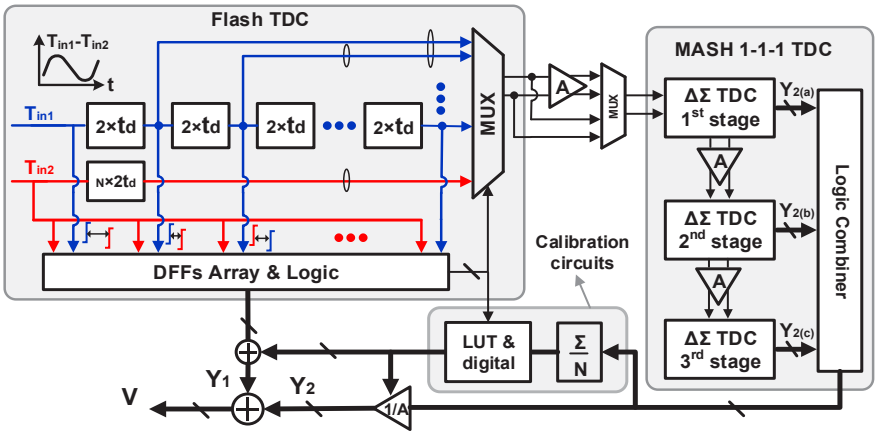

Fig. 4: Block diagram of TA based two-step flash-ΔΣ TDC with calibration circuits.

Fig. 3(b) shows further details of the 1st order ΔΣ TDC. The ΔΣ TDC runs at its full speed F_S=50MHz while the de-multiplexer delivers the input samples to the two-parallel time registered subtractors, whose operational frequency is reduced to $F_S/2$=25 MHz. Then, the multiplexer sequentially selects the output of each channel to obtain 50 MHz, i.e., the full rate output. A 3-bit bi-direction TDC (processes positive/negative input) with resolution of $2\times t_d$ (20 ps) is used to work as both TDC and DTC. The DFFs array detects the critical residue and then the multiplexer feeds it back to the input. The time residue is also amplified and fed into the next-stage ΔΣ TDC. The ×8 TA is realized by cascading three time adders which are clocked by 3×Fs.

C. TA based flash-ΔΣ MASH 1-1-1 TDC with calibration

The block diagram of the TA-based two-step flash-ΔΣ TDC is shown in Fig. 4. The 1st stage 4-bit flash TDC with $2\times t_d$ delay-time buffers (t_d is equivalent to the inverter delay) quantizes the input time difference while the multiplexer determines which one of the residues is amplified and sent to the 2nd stage. A $2N\times t_d$ delay on the input path is used to compensate for the latency of residue generation.

A calibration circuit including a look-up table (LUT) and an averaging circuit is implemented to store the digitized delay time of the flash TDC. The delay time of each delay cell is sequentially sent to the fine resolution ΔΣ TDC for quantization (without amplification). The averaged output of ΔΣ TDC is chosen to store in the LUT. The gain offset of TA can also be calibrated by the ΔΣ TDC. After the flash TDC calibration the already known delay time of a delay cell is passed through the TA. The quantized output is averaged to adjust the scale factor of 1/A.

IV. Simulation Results

A. Nonlinearity of flash-ΔΣ TDC

Fig. 5(a) shows the PSDs of TDC output with different amplifications. The quantization noise is reduced by increasing the gain of amplifiers. A ×8 amplification can reduce the quantization noise below the device noise. The ΔΣ TDC behaves like a flash TDC whose noise has a flat noise characteristic. Considering the mismatch caused by the 1st flash TDC, the Fig. 5(b) illustrates the PSDs with and without 5% delay error of Gaussian distribution. The nonlinearity will generate the 'unexpected' spurious tones, which will decrease the noise performance.

As shown in Fig. 5(c), the gain offset will also cause the spurious tones, however, the offset caused by the TA, which is located between the 1st and 2nd TDCs, is more critical than the others in the ΔΣ TDC stages since the nonlinearity in ΔΣ TDC is already scaled by its preceding TA. Therefore, the calibration only needs to be applied to the flash TDC and the 1st-to-2nd stage TA. The calibration methods which are used in Section III can achieve 99.8% accuracy by averaging 1000 samples. Fig. 5(d) shows the PSDs before and after calibration.

B. Performance of proposed TDC

The TA-based two-step flash-ΔΣ TDC is implemented in 40-nm CMOS. The simulated output power spectral density with a 28kHz 124ps peak-to-peak sinusoidal input and F_S=50 MHz is depicted in Fig. 6. It is clearly evident that the 1/f flicker noise and thermal noise dominate at low frequencies. The measured integrated noise within Nyquist bandwidth, 25MHz is equal to -39.6dB, which translates to $143fs_{rms}$. To achieve the same integrated noise level with the same sampling frequency, but assuming white noise PSD, it yields the equivalent flash-TDC step of Δt_{res}=0.5 ps. The TDC current consumption is 1.3 mA with 1.1 V supply at 50 MHz.

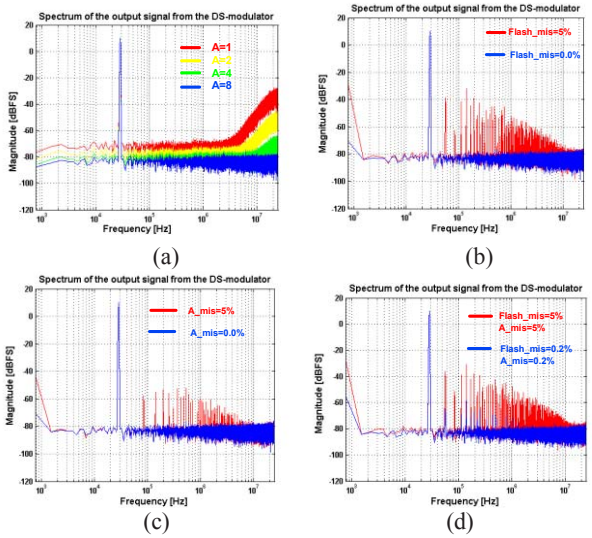

Fig. 5: PSDs of TDC output with: different amplifications (a); ideal flash-TDC delay and 5% mismatch (b); ideal amplification and 5% gain offset (c); 5% and 0.2% flash-TDC delay and gain offset (d).

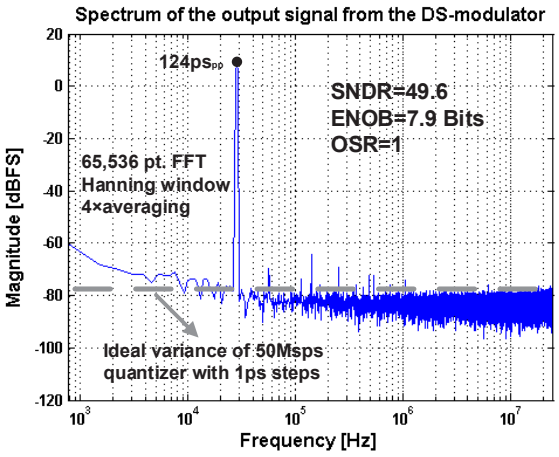

Fig. 6: Simulated PSD of TDC output.

In order to simulate the linearity performance of the proposed TDC, a time-domain ramp input sequence is applied to the TDC by two clock generators whose frequencies are slightly different, such as 50MHz and 49.9998MHz. Fig. 7 shows simulated TDC output after 2^{15} samples are collected. The maximum INL obtained is equal to ±0.01 LSB/20ps or ±0.2ps.

V. Conclusions

We have proposed a TA-based two-step flash-ΔΣ TDC where the 2nd stage works in a MASH 1-1-1 fashion. The simulated TDC displays a flat noise and archives 143 fs integrated noise or 0.5 ps equivalent resolution within Nyquist bandwidth. Operating at a 50 MHz sampling frequency, the current consumption of the TDC is 1.3 mA from 1.1 V.

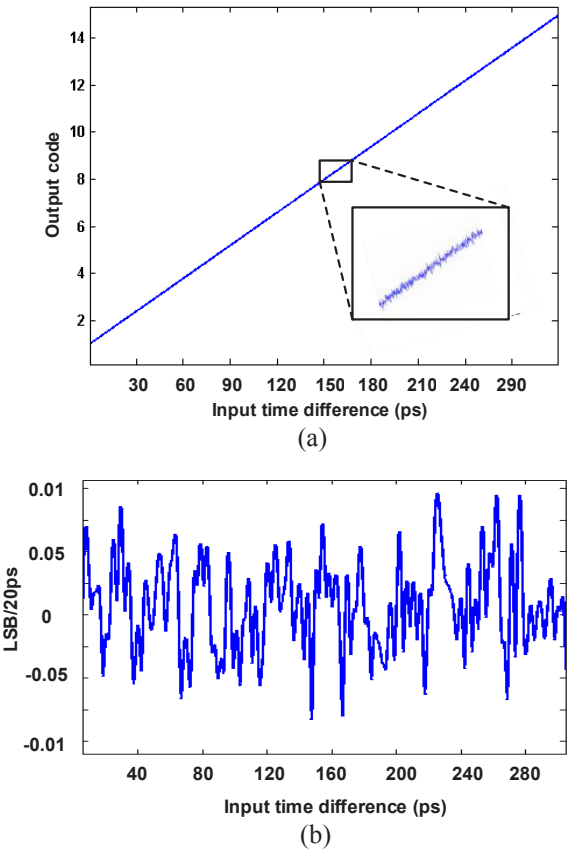

Fig. 7 Simulated TDC output for a ramp input (a); INL(b).

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